ANT-20, ANT-20E
Advanced Network Tester

M13 MUX/DEMUX

BN 3035/90.32

Drop & Insert

BN 3035/90.20
in combination with
M13 MUX/DEMUX

Software Version 7.20

Operating Manual

5

BN 3035/98.24

WAVETEK
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Communications Test Solutions

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Contents

Introduction

Option BN 3035/90.32

1 Multiplex and demultiplex functions

When equipped with Option BN 3035/90.32, “M13 MUX/DEMUX”, the ANT-20 can generate and analyze DS3 signals containing 28 DS1 signals. These DS3 signals can also be mapped into OC-N signals or STM-N and STS-N signals. This allows tests on add/drop multiplexers equipped with built-in M13 multiplexs or on M13 signals. It is also possible to insert an external DS1 signal via a connector ot to drop an internal DS1 signal and output it via a connector (Drop & Insert Option, BN 3035/10.20).

The appropriate signal structures are set in the “Signal Structure” window using the “Signal Structure Editor”.

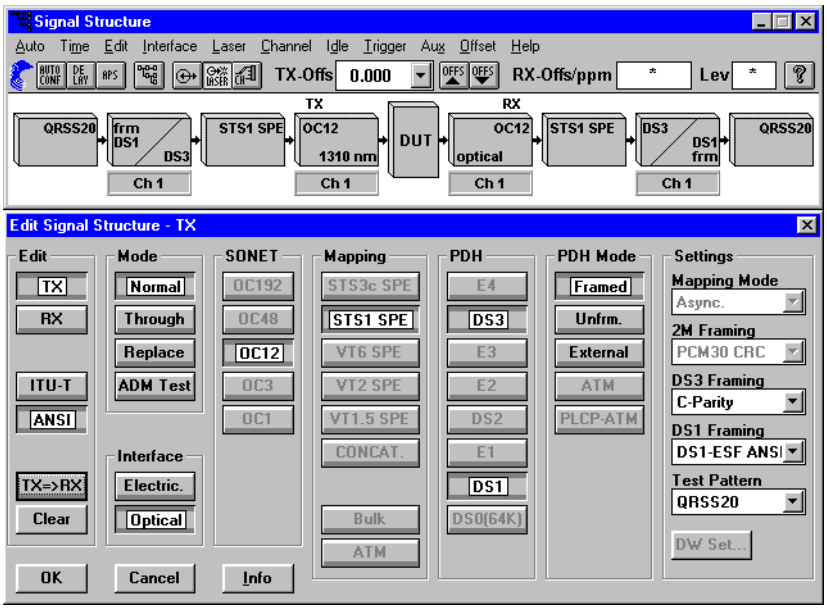

Fig. I-1 Testing an add/drop multiplexer (ADM) equipped with M13 multiplexer

2 Testing switch and sensor functions

Switch functions

SONET network elements process asynchronous (DSn) signals of various hierarchy levels. Complex, interleaved signal paths occur, particularly in modern SDH network nodes (cross-connects). The linking of the M13 multiplex function to the SONET mapping functions in the ANT-20 makes the instrument ideal for testing complex switching functions.Tests can be performed between two SONET ports, two DSn ports or between a SONET and a DSn port.

Alarm sensor test

Comprehensive facilities for inserting errors at the DS1 and DS3 levels allow testing of the monitor functions built in to the network elements. This is particularly useful during installation work, as the network management systems are dependent on the correct functioning of these sensors during subsequent operation.

3 In-service monitoring of tributary channels

The demultiplex function provides access to the tributary channels right down to the DS1 level. This permits pinpoint in-service monitoring of individual channels in DSn signals and in SONET signals when the appropriate mappings are employed.

Specifications

Option BN 3035/90.32

1 Generator section

1.1 Frame generator, M13 MUX/DEMUX (option BN 3035/90.32)

The following frames are available:

Level	Bit rate in kbit/s	Frames conforming to	Notes
DS1	1544	T1.107	SF (D4)
	1544	T1.107	ESF (T1.107)
DS2	6312	T1.107	-
DS3	44736	T1.107	M13
	44736	T1.107a	C parity

Table S-1 Frame generation

The multiplexer chain (BN 3035/90.32) allows generation of a completely structured signal with 28 DS1 signals in a DS3 signal.
The DS2 level cannot be manipulated.

1.2 CRC checksum (DS1 ESF)

The ANT-20 calculates the CRC-6 checksum for the measured channel and the filler channels as per standard T1.107 and inserts the result bits at the appropriate position in the Extended Super Frame.

1.3 Justification as per T1.107 or T1.107a

The bit rates in the upper and subordinate systems are in a fixed relationship to each other.

Justification is at a nominal rate (offset of upper and subordinate systems is identical). Exception: Insertion of external signals.

M13

Upper system	Justification ratio	Justification rate in kbit/s
DS2	0.335	1.8
DS3	0.39	3.544

Table S-2 M13 justification

C parity

Upper system	Justification ratio	Justification rate in kbit/s
DS2	0.073	0.393
DS3	1	9.398

Table S-3 C parity justification

1.3.1 PDH tributary offset

Static offset for the PDH tributary bit rates during insertion into the SONET-SPE container.

Offset . . . . . ±100 ppm
for all bit rates, relative to SONET-SPE container
Step width . . . . . 1 ppm

The offset is an average value. The actual offset at any given time may be above or below this value.

1.4 Error insertion (anomalies)

The error types are described in the “Specifications” for the mainframe instrument.

1.5 Alarm generation (defects)

The alarm types are described in the “Specifications” for the mainframe instrument.

The insertion of **alarms** (defects) **or errors** (anomalies) are mutually exclusive. The action selected first is active.

1.6 Test signals for bit error rate measurements

1.6.1 Internal test signals

Bit patterns as in the mainframe instrument:

- Transmitted in all timeslots (framed pattern)
- Transmitted in a selected timeslot

1.6.2 External signal (with option 3035/90.20 only)

An external signal with bit rate 1544 kbit/s (coaxial or balanced) can be inserted into the selected timeslot instead of the bit pattern (see Sec. 1.6.1).

The interfaces for this signal are described in Sec. 3, Page S-6.

1.6.3 Filler signals

Complete structured signals using the pseudo-random bit sequence PRBS 6 are transmitted in all 64 kbit/s channels.

2 Receiver section

2.1 Frame systems

Frames which can be evaluated by the M13 MUX/DEMUX chain (Option BN 3035/90.32):

Level	Bit rate in kbit/s	Frames conforming to	Notes
DS1	1544	T1.107	SF (D4)
	1544	T1.107	ESF (T1.107)
DS2	6312	T1.107	-
DS3	44736	T1.107	M13
	44736	T1.107a	C parity

Table S-4 Frame systems for individual system bit rates

One channel is selected as test channel from the 28 DS1 signals.
The DS2 level cannot be evaluated.

2.2 Error measurements (anomalies)

The error measurements are described in the “Specifications” for the mainframe instrument. The frame alignment signals in all hierarchy stages of the selected path are checked simultaneously.

2.3 Alarm detection (defects)

The detected alarms are described in the “Specifications” for the mainframe instrument. The RDI alarms (yellow) in all hierarchy stages of the selected path are checked simultaneously.

2.4 Offset measurements

All offsets in the hierarchy stages of the selected path are measured and displayed simultaneously.

Display in ppm

2.5 Evaluation of test signals for bit error measurements

2.5.1 Internal evaluation

Evaluation:

- in all timeslots (framed pattern)
- in the selected timeslot

2.5.2 External signal (with option BN 3035/90.20 only)

Output of a signal with bit rate 1544 kbit/s (coaxial or balanced) for external evaluation is alternative to internal evaluation as described before (see Sec. 2.5.1).

The interfaces for this are described in Sec. 3, Page S-6.

3 Drop&Insert / Through Mode / Block&Replace

Option BN 3035/90.20

3.1 Functions

This option provides the following functions for all mapping options fitted to the ANT-20.

Drop&Insert

Generator and receiver operate independently as multiplexer and demultiplexer. The signal from a selected tributary is dropped from the receive signal and output to a connector. An external signal is inserted into the transmit signal.

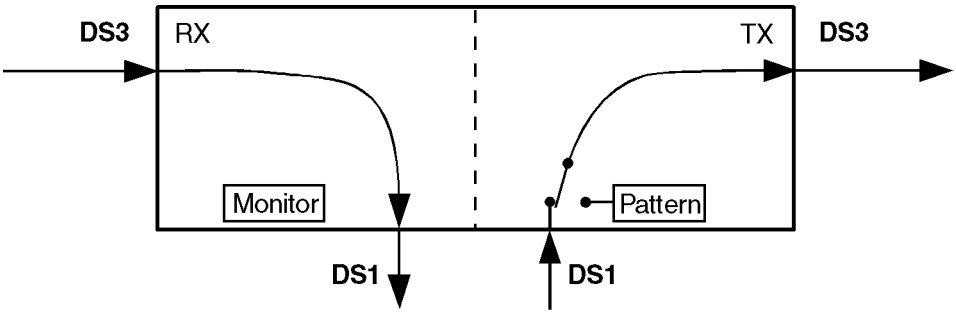

Fig. S-1 Drop&Insert: Generator and receiver operate independently

An unbalanced digital input and output are provided on the mainframe instrument for dropping and for inserting tributary signals (see Sec. 3.2.1, Page S-8 and Sec. 3.3.1, Page S-9).

The mainframe instrument is also equipped with a balanced output [13] and input [12] for dropping and for inserting tributary signals via balanced interfaces

Through Mode

The received signal is looped through the ANT-20 and re-transmitted by the generator.

The ANT-20 operates in Through Mode as a signal monitor without affecting the signal content.

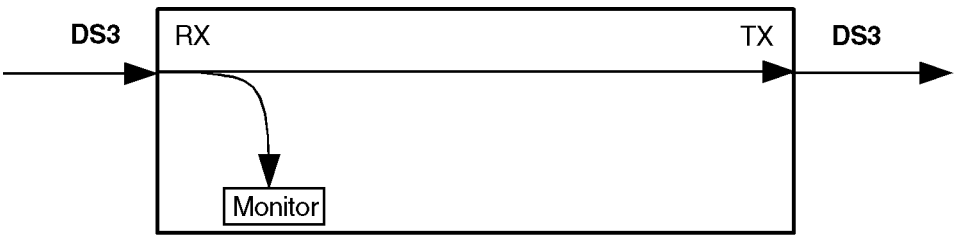

Fig. S-2 Through Mode: Generator and receiver coupled

The looped-through signal can also be jittered using the Jitter Generator options (Jitter Generator up to 155 or 622 Mbit/s, BN 3035/90.60 to 61). This function is available for all bit rates fitted to the instrument.

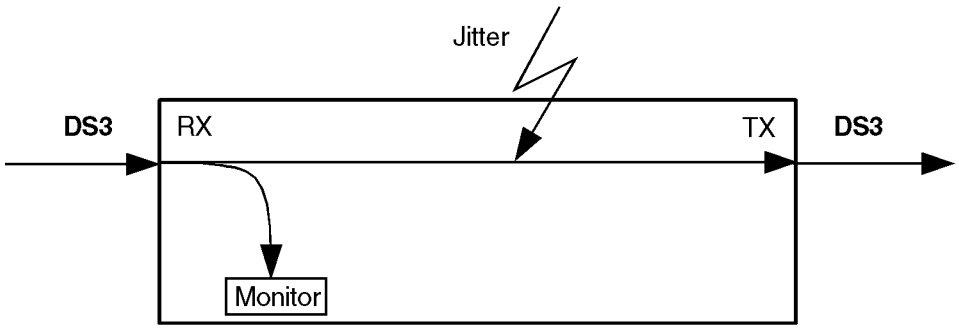

Fig. S-3 Through Mode: Adding jitter to the looped-through signal

Block&Replace

In PDH mode not possible.

3.1.1 Clock generator

Drop&Insert

As specified in the “Specifications” of the mainframe instrument.

Through Mode

In Through Mode, clock generation is always derived from the receive signal clock. No signal offset is possible in this operating mode (see also the “Specifications” of the mainframe instrument).

3.1.2 Anomaly insertion

Drop&Insert

As specified in Sec. 1.4, Page S-2.

Through Mode

Anomaly insertion is not possible.

3.1.3 Defect generation

Drop&Insert

As specified in Sec. 1.5, Page S-2.

Through Mode

Defect generation is not possible.

3.1.4 Measurements

There are no restrictions on measurements (see Sec. 2, Page S-4).

3.2 Signal outputs

3.2.1 AUXILIARY signal output [11], electrical

Connector . . . . . unbalanced, (coaxial)

Socket type . . . . . BNC

Output impedance . . . . . 75 Ω

Max. permitted peak spurious input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Output voltage
E4	139.264	CMI	± 0.5 V
DS3	44.736	B3ZS	± 1.0 V
E3	34.368	HDB3	
E2	8.448	HDB3	± 2.37 V
E1	2.048	HDB3	
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-5 Specifications of the AUXILIARY signal output [11], electrical

3.2.2 LINE/AUXILIARY signal output [13], electrical

Connector . . . . . balanced

Socket type . . . . . Lemo SA (Bantam)

Output impedance
2.048 Mbit/s . . . . . 120 Ω
1.544 Mbit/s . . . . . 100 Ω

Max. permitted peak spurious input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Output voltage
E1	2.048	HDB3	± 3.0 V
DS1	1.544	B8ZS	DSX-1 compatible
The bit rates depend on the mapping options fitted.			

Table S-6 Specifications of the LINE/AUXILIARY signal output [13], electrical

The balanced output is used as a LINE or as an AUXILIARY output.

3.3 Signal inputs

3.3.1 AUXILIARY signal input [10], electrical

Connector . . . . . unbalanced, (coaxial)

Socket type . . . . . BNC

Input impedance . . . . . 75 Ω

Max. permitted frequency offset . . . . . ± 500 ppm

Input voltage range . . . . . 0 dB attenuation referred to nominal level

Max. permitted peak input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Input voltage
E4	139.264	CMI	1.0 V ±10 %
DS3	44.736	B3ZS	1.0 V ±10 %
E3	34.368	HDB3	
E2	8.448	HDB3	2.37 V ±10 %
E1	2.048	HDB3	
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-7 Specifications of the AUXILIARY signal input [10], electrical

LOS (Loss of Signal) status display

LED lights up if the signal input is active but no signal is present.

3.3.2 LINE/AUXILIARY signal input [12], electrical

Connector . . . . . balanced

Socket type . . . . . Lemo SA (Bantam)

Input impedance
2.048 Mbit/s . . . . . 120 Ω
1.544 Mbit/s . . . . . 100 Ω

Max. permitted frequency offset . . . . . ± 500 ppm

Max. number of consecutive zeros for line code = AMI 15

Max. permitted peak input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Input voltage
E1	2.048	HDB3	3.0 V ±10 %
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-8 Specifications of the LINE/AUXILIARY signal input [12], electrical

LOS (Loss of Signal) status display

LED lights up if the signal input is active but no signal is present.

The balanced input is used as a LINE or as an AUXILIARY input.